CE65H160DNDI

CoreGaN 650V GaN HEMT

Description

The CE65H160DNDI Series 650V, 160mΩ gallium nitride (GaN) FETs are normally-off devices.

Corenergy GaN FETs offer better efficiency through lower gate charge, faster switching speeds, and lower dynamic on-resistance, delivering significant advantages over traditional silicon (Si) devices.

Corenergy is a leading-edge wide band gap supplier with world-class innovation .

Application

- Adapter
- Renewable energy
- Telecom and data-com
- Servo motors
- Industrial
- Automotive

General Features

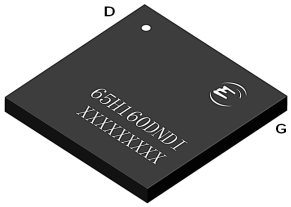
Easy to drive—compatible with standard gate drivers

Low conduction and switching losses

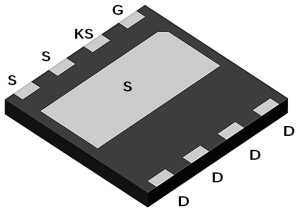
RoHS compliant and Halogen-free

Ordering Information

Part Number	Package	Package Configuration
CE65H160DNDI	DFN 8*8	Source



Top



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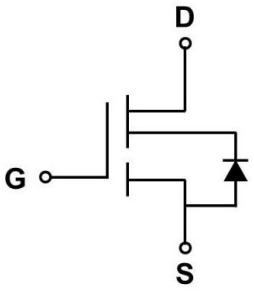

Circuit Symbol

Benefits

Increased efficiency through fast switching

Increased power density

Reduced system size and weight

Features

BV_{DSS}	R_{DSON}	I_{DS}	Q_G
650V	160mΩ	14.5A	7.4nC

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Absolute Maximum Ratings

T_C=25°C unless otherwise stated

Symbol	Parameter		Limit value	Unit
V_{DSS}	Drain to source voltage (T_J = -55°C to 150°C)		650	V
$V_{(TR)DSS}$	Drain to source voltage-transient [a]		800	
V_{GSS}	Gate to source voltage		-20~+20	
I_D	Continuous drain current @T_C=25°C [b]		14.5	A
	Continuous drain current @T_C=125°C [b]		6.4	
I_{DM}	Pulse drain current (pulse width: 10μs)		27	A
P_D	Maximum power dissipation @ T_C=25°C		89	W
T_C	Operating temperature	Case	-55~150	°C
T_J		Junction	-55~150	°C
T_S	Storage temperature		-55~150	°C

a. In off-state, spike duty cycle D<0.01, spike duration <1μs

b. For increased stability at high current operation

Thermal Resistance

Symbol	Parameter	Limit value	Unit
$R_{\theta JC}$	Junction-to-case	1.4	°C /W

CE65H160DNDI

Electrical Parameters

T_J=25°C unless otherwise stated

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Forward Device Characteristics						
$V_{(BL)DSS}$	Drain-source voltage	650	-	-	V	V_{GS}= 0V
$V_{GS(th)}$	Gate threshold voltage	3.3	3.9	4.5	V	V_{DS}=1V, I_{DS}=1mA
$\triangle V_{GS(th)}/T_J$	Gate threshold voltage temperature coefficient	-	-7	-	mV/°C	
$R_{DS(on)}$	Drain-source on-Resistance	-	160	200	mΩ	V_{GS}=10V, I_D=1A, T_J=25°C
		-	350	-		V_{GS}=10V, I_D=1A, T_J=150°C
I_{DSS}	Drain-to-source leakage current	-	1	10	μA	V_{DS}=650V, V_{GS}= 0V, T_J=25°C
		-	5	100		V_{DS}=650V, V_{GS}= 0V, T_J=150°C
I_{GSS}	Gate-to-source forward leakage current	-	-	±100	nA	V_{GS}=±20V
C_{ISS}	Input capacitance	-	329	-	pF	V_{GS}=0V, V_{DS}=400V, f=1MHz
C_{OSS}	Output capacitance	-	25	-		
C_{RSS}	Reverse capacitance	-	1	-		
Q_G	Total gate charge	-	7.4	-	nC	V_{DS}=400V, V_{GS}=0V to 10V, I_D=1A
Q_{GS}	Gate-source charge	-	2.6	-		
Q_{GD}	Gate-drain charge	-	1.8	-		
Q_{OSS}	Output charge	-	34	-	nC	V_{GS}=0V, V_{DS}=0V to 400V, f=1MHz
$t_{D(on)}$	Turn-on delay	-	3.3	-	ns	V_{DS}=400V, V_{GS}=0V to 10V, I_D=2.1A, $R_{G-on(ext)}$=6.8Ω, $R_{G-off(ext)}$=2.2Ω, L=250μH
t_R	Rise time	-	7	-		
$t_{D(off)}$	Turn-off delay	-	9.8	-		
t_F	Fall time	-	27	-		

Electrical Parameters

T_J=25°C unless otherwise stated

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Reverse Device Characteristics						
V_{SD}	Source-Drain reverse voltage	-	2.5	-	V	V_{GS}=0V, I_{SD}=10A
t_{RR}	Reverse recovery time	-	14	-	ns	I_F=10A, V_{DD}=400V, dI_F/dt=165A/μs
Q_{RR}	Reverse recovery charge	-	6.5	-	nC	

Typical Characteristics

T_J=25°C unless otherwise stated

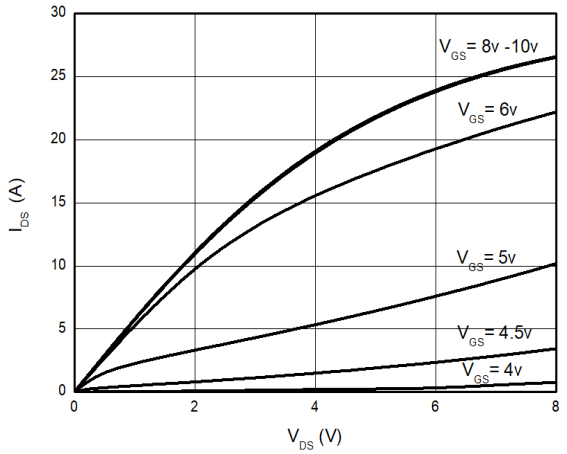

Figure 1. Typical Output Characteristics T_J=25°C

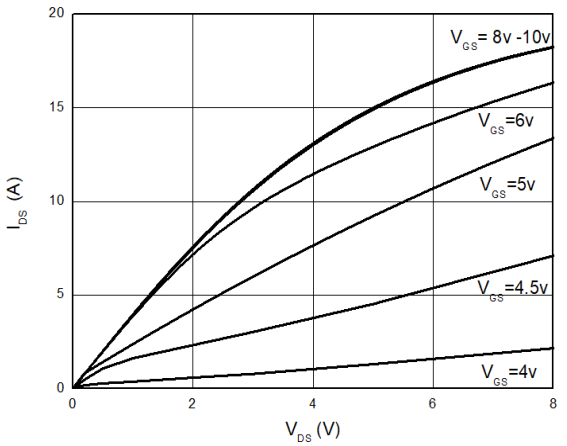

Figure 2. Typical Output Characteristics T_J=125°C

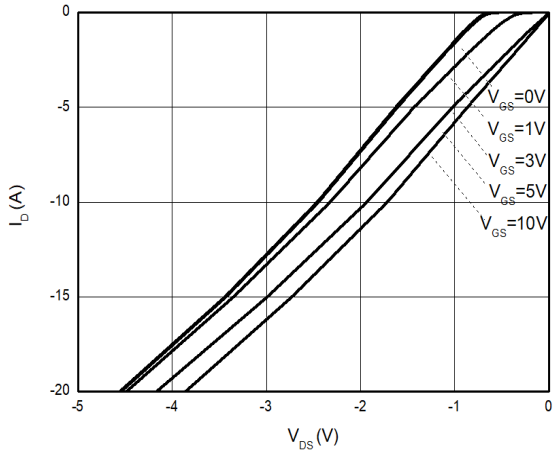

Figure 3. Channel Reverse Characteristics T_J=25°C

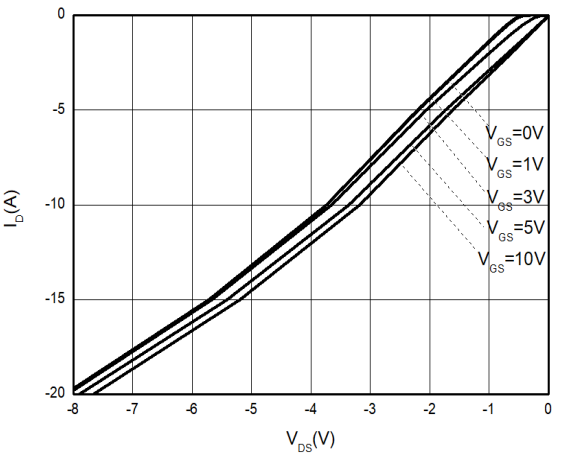

Figure 4. Channel Reverse Characteristics T_J=125°C

Typical Characteristics

T_J=25°C unless otherwise stated

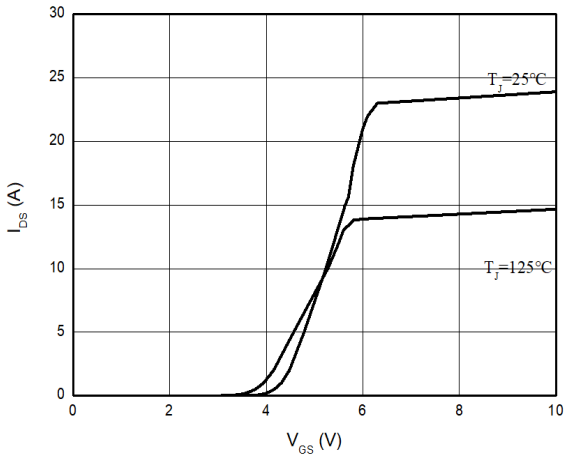

Figure 5. Typical Transfer Characteristics (V_{DS}=5V)

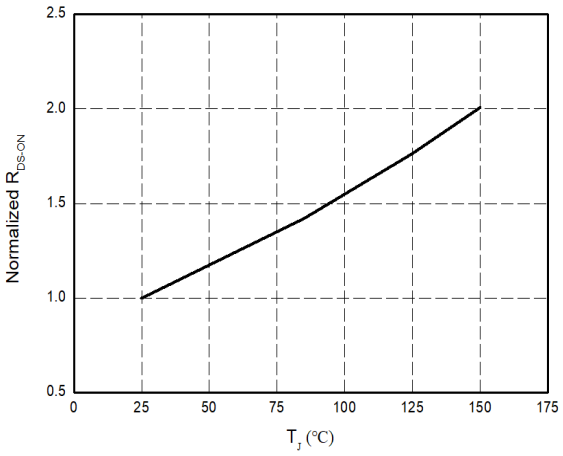

Figure 6. Normalized On-resistance

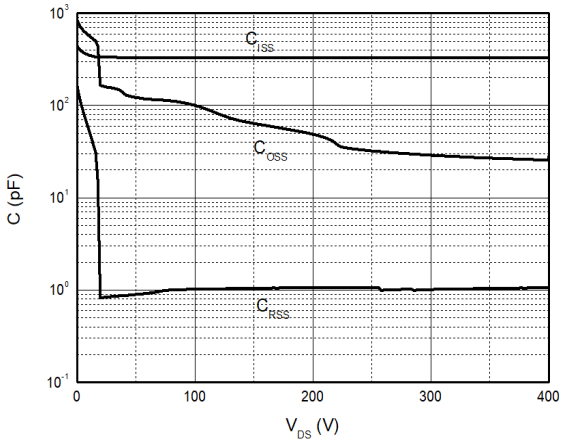

Figure 7. Typical Capacitance (f=1MHz)

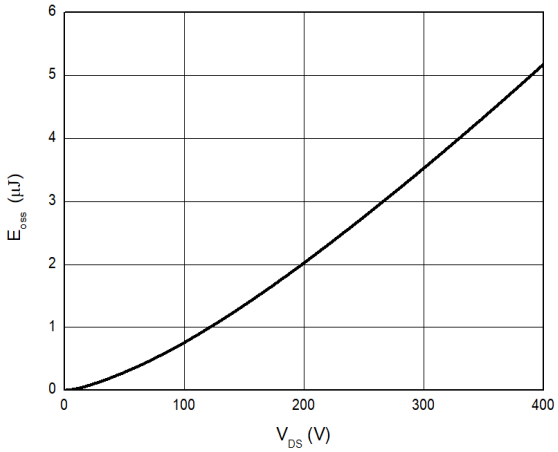

Figure 8. Typical C_{OSS} Stored Energy

Typical Characteristics

T_J=25°C unless otherwise stated

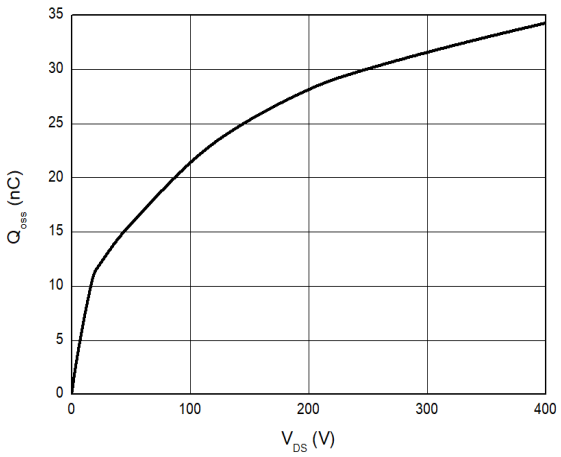

Figure 9. Typical Q_{OSS}

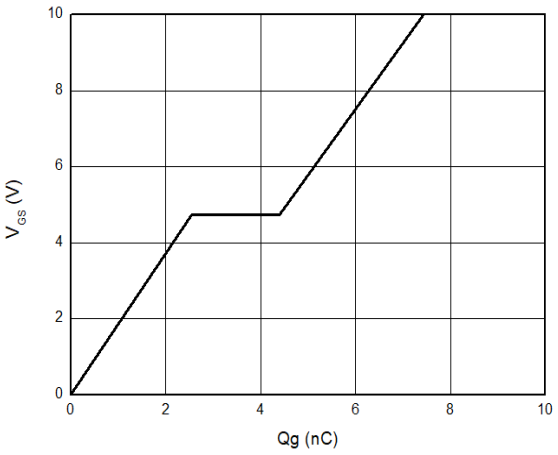

Figure 10. Typical Gate Charge (V_{DS}=400V, I_D=1A)

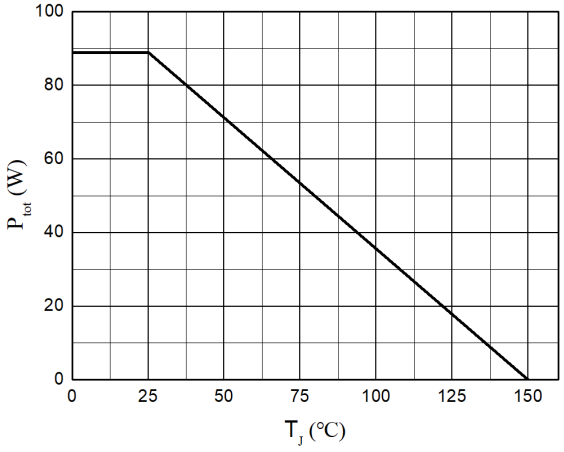

Figure 11. Power Dissipation

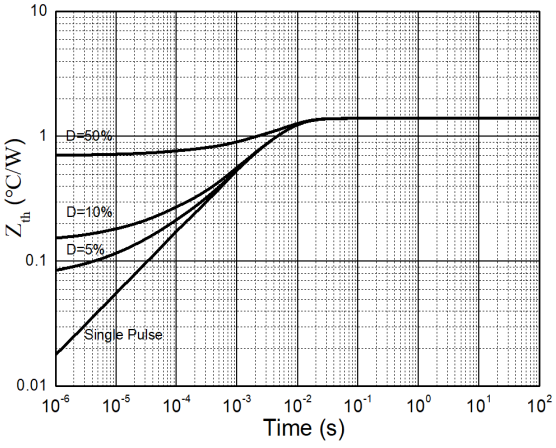

Figure 12. Transient Thermal Resistance

Typical Characteristics

T_J=25°C unless otherwise stated

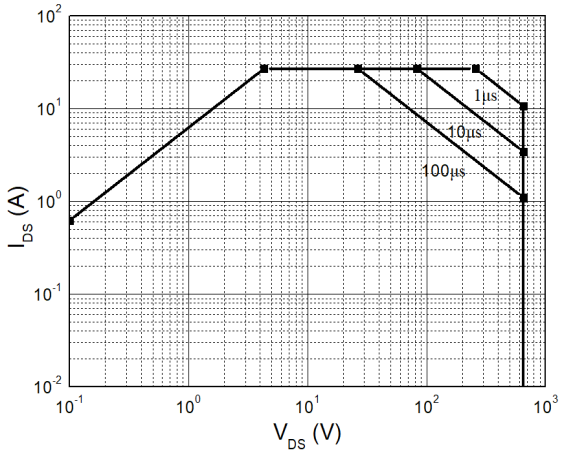

Figure 13. Safe Operating Area T_C=25°C

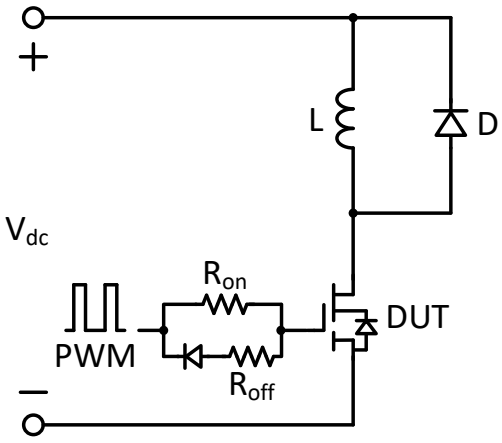

Figure 14. Switching times with inductive load

V_{DS}=400V, V_{GS}=0V to 10V, I_D=2.1A, $R_{G\text{-}on(ext)}$=6.8Ω, $R_{G\text{-}off(ext)}$=2.2Ω, L=250μH

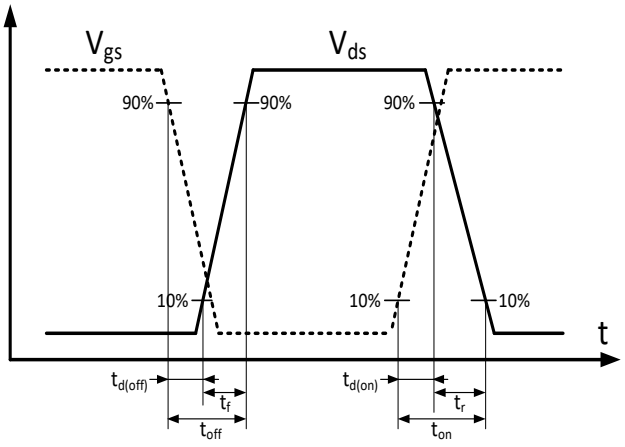

Figure 15. Switching times with waveform

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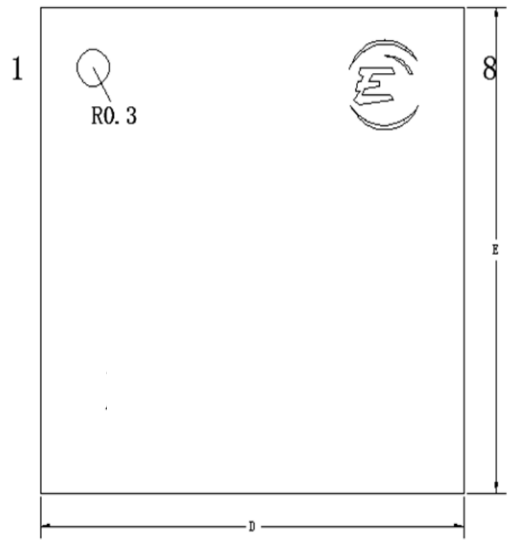
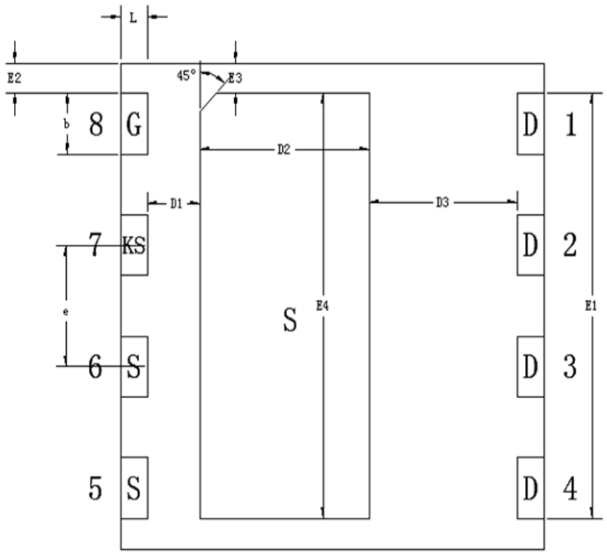
PACKAGE DIMENSIONS

DFN8x8-8L-1.10-A

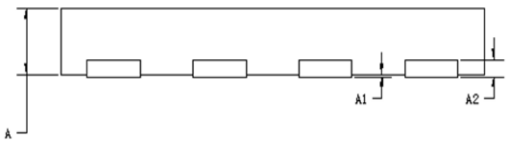
Top view



Bottom view



Side view(left/right)



Symbol	Min. (mm)	Mean. (mm)	Max. (mm)
A	1.05	1.10	1.15
A1	0	0.02	0.05
A2		0.203REF	
D	7.9	8	8.1
E	7.9	8	8.1
D1	0.9	1	1.1
D2	3.1	3.2	3.3
D3	2.7	2.8	2.9
E1	6.9	7	7.1
E2	0.4	0.5	0.6
E3	0.4	0.5	0.6
E4	6.9	7	7.1
e	1.9	2	2.1
b	0.9	1	1.1
L	0.4	0.5	0.6

Revision history

Major changes since the last revision

Revision	Date	Description of changes
1.0	2022-02-28	Initial release
2.0	2024-06-01	Enrich dynamic specification curves