



CE65H160DNXI

CoreGaN 650V GaN HEMT

Description

The CE65H160DNXI Series 650V, 160mΩ gallium nitride (GaN) FETs are normally-off devices.

Coreenergy GaN FETs offer better efficiency through lower gate charge, faster switching speeds, and lower dynamic on-resistance, delivering significant advantages over traditional silicon (Si) devices.

Coreenergy is a leading-edge wide band gap supplier with world-class innovation .

Application

- Adapter
- Renewable energy
- Telecom and data-com
- Servo motors
- Industrial
- Automotive

General Features

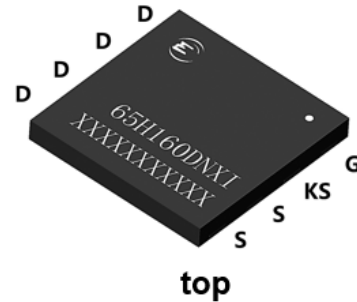
Easy to drive—compatible with standard gate drivers
 Low conduction and switching losses
 RoHS compliant and Halogen-free

Benefits

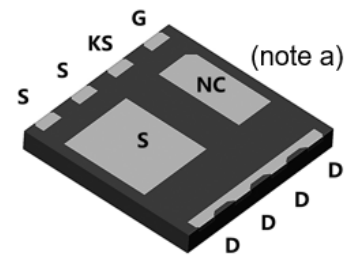
Increased efficiency through fast switching
 Increased power density
 Reduced system size and weight

Ordering Information

Part Number	Package	Package Configuration
CE65H160DNXI	DFN 8*8	Source



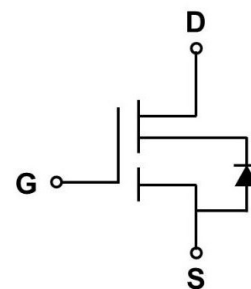
top



bottom

Note :

- a. NC solder pad represents GaN source & MOS Drain; The electrical connection is prohibited.



Circuit Symbol

Features

BV_{DSS}	$R_{DS(on)}$	I_{DS}	Q_G
650V	160mΩ	12.7A	7.4nC



Absolute Maximum Ratings

$T_c=25^\circ\text{C}$ unless otherwise stated

Symbol	Parameter	Limit value	Unit	
V_{DSS}	Drain to source voltage ($T_J = -55^\circ\text{C}$ to 150°C)	650		
$V_{(TR)DSS}$	Drain to source voltage-transient ^a	800	V	
V_{GSS}	Gate to source voltage	-20~+20		
I_D	Continuous drain current @ $T_c=25^\circ\text{C}$ ^b	12.7	A	
	Continuous drain current @ $T_c=125^\circ\text{C}$ ^b	5.7		
I_{DM}	Pulse drain current (pulse width: 10 μs)	27	A	
P_D	Maximum power dissipation @ $T_c=25^\circ\text{C}$	68	W	
T_c	Operating temperature	Case	-55~150	$^\circ\text{C}$
T_J		Junction	-55~150	$^\circ\text{C}$
T_S	Storage temperature	-55~150	$^\circ\text{C}$	

Notes:

a. In off-state, spike duty cycle $D < 0.01$, spike duration $< 1\mu\text{s}$

b. For increased stability at high current operation



Thermal Resistance

Symbol	Parameter	Limit value	Unit
$R_{\theta JC}$	Junction-to-case	1.82	$^{\circ}\text{C} / \text{W}$



Electrical Parameters

$T_J=25^\circ\text{C}$ unless otherwise stated

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Forward Device Characteristics						
$V_{(BL)DSS}$	Drain-source voltage	650	-	-	V	$V_{GS}=0V$
$V_{GS(th)}$	Gate threshold voltage	3.3	3.9	4.5	V	$V_{DS}=1V, I_{DS}=1mA$
$\Delta V_{GS(th)}/T_J$	Gate threshold voltage temperature coefficient	-	-7	-	mV/°C	
$R_{DS(on)}$	Drain-source on-Resistance	-	160	210	mΩ	$V_{GS}=10V, I_D=1A, T_J=25^\circ\text{C}$
		-	340	-		$V_{GS}=10V, I_D=1A, T_J=150^\circ\text{C}$
I_{DSS}	Drain-to-source leakage current	-	1	10	μA	$V_{DS}=650V, V_{GS}=0V, T_J=25^\circ\text{C}$
		-	5	100		$V_{DS}=650V, V_{GS}=0V, T_J=150^\circ\text{C}$
I_{GSS}	Gate-to-source forward leakage current	-	-	±100	nA	$V_{GS}=\pm 20V$
C_{ISS}	Input capacitance	-	330	-	pF	$V_{GS}=0V, V_{DS}=400V, f=1MHz$
C_{OSS}	Output capacitance	-	25	-		
C_{RSS}	Reverse capacitance	-	1	-		
Q_G	Total gate charge	-	7.4	-	nC	$V_{DS}=400V, V_{GS}=0V \text{ to } 10V, I_D=1A$
Q_{GS}	Gate-source charge	-	2.6	-		
Q_{GD}	Gate-drain charge	-	1.8	-		
Q_{OSS}	Output charge	-	34	-	nC	$V_{GS}=0V, V_{DS}=0V \text{ to } 400V, f=1MHz$
$t_{D(on)}$	Turn-on delay	-	3.3	-	ns	$V_{DS}=400V, V_{GS}=0V \text{ to } 10V, I_D=2.1A,$ $R_{G-on(ext)}=6.8\Omega, R_{G-off(ext)}=2.2\Omega,$ $L=250\mu H$
t_R	Rise time	-	7	-		
$t_{D(off)}$	Turn-off delay	-	9.8	-		
t_F	Fall time	-	27	-		



Electrical Parameters

$T_j=25^\circ\text{C}$ unless otherwise stated

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Reverse Device Characteristics						
V_{SD}	Source-Drain reverse voltage	-	2.5	-	V	$V_{GS}=0\text{V}$, $I_{SD}=10\text{A}$
t_{RR}	Reverse recovery time	-	14	-	ns	$I_F=10\text{A}$, $V_{DD}=400\text{V}$, $di_F/dt=165\text{A}/\mu\text{s}$
Q_{RR}	Reverse recovery charge	-	6.5	-	nC	



Typical Characteristics

$T_j=25^\circ\text{C}$ unless otherwise stated

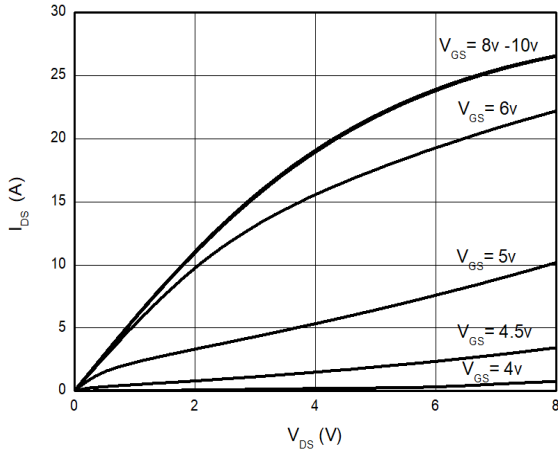


Figure 1. Typical Output Characteristics $T_j=25^\circ\text{C}$

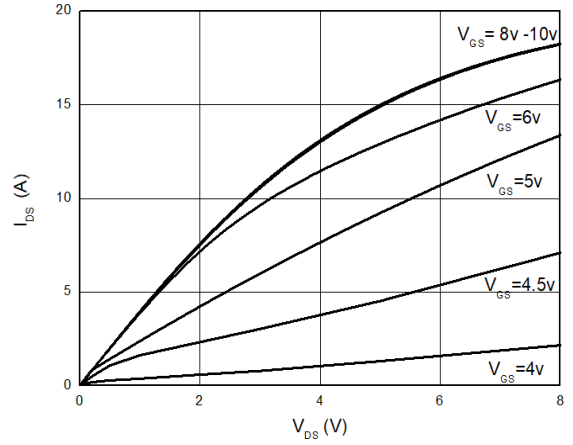


Figure 2. Typical Output Characteristics $T_j=125^\circ\text{C}$

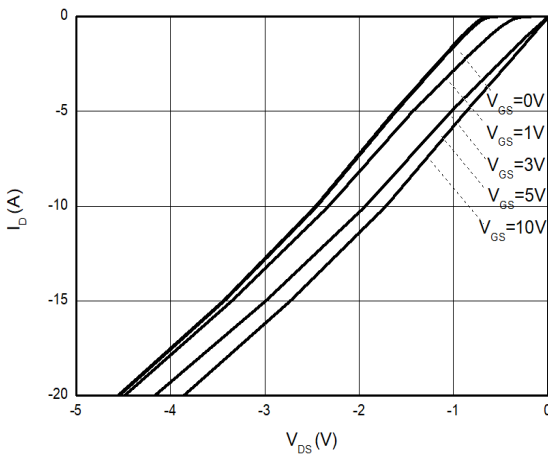


Figure 3. Channel Reverse Characteristics $T_j=25^\circ\text{C}$

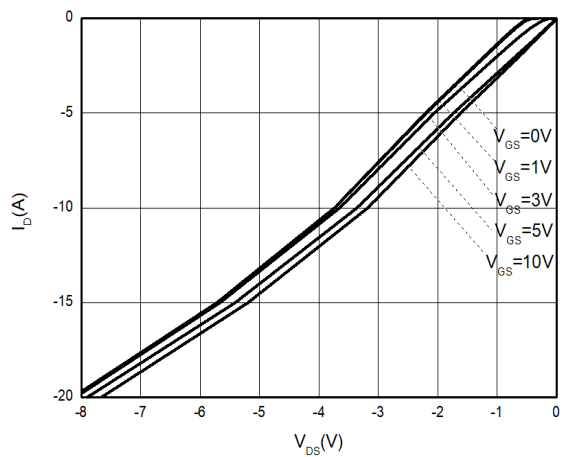


Figure 4. Channel Reverse Characteristics $T_j=125^\circ\text{C}$



Typical Characteristics

$T_j=25^\circ\text{C}$ unless otherwise stated

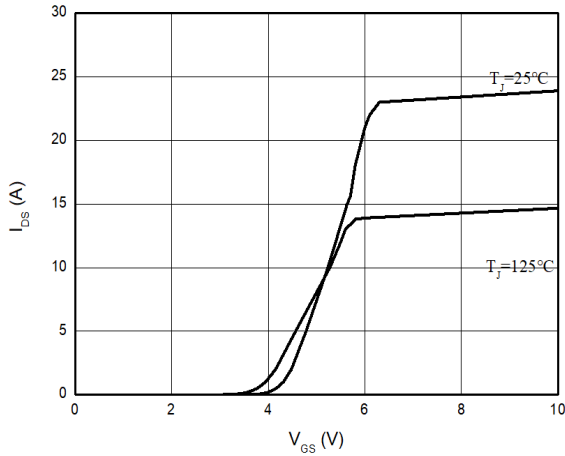


Figure 5. Typical Transfer Characteristics ($V_{DS}=10V$)

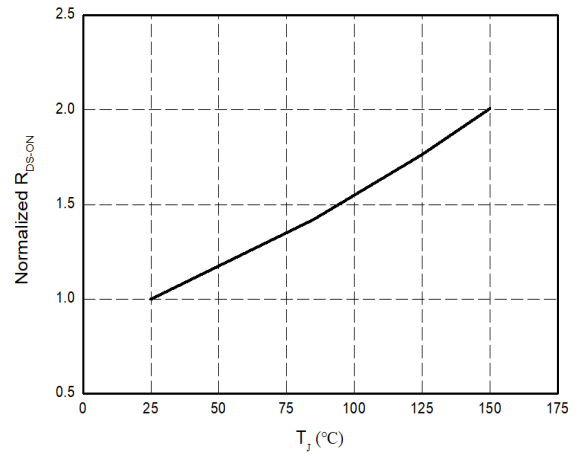


Figure 6. Normalized On-resistance

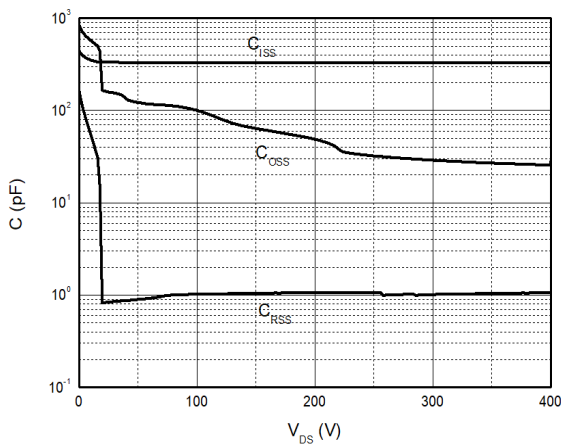


Figure 7. Typical Capacitance ($f=1\text{MHz}$)

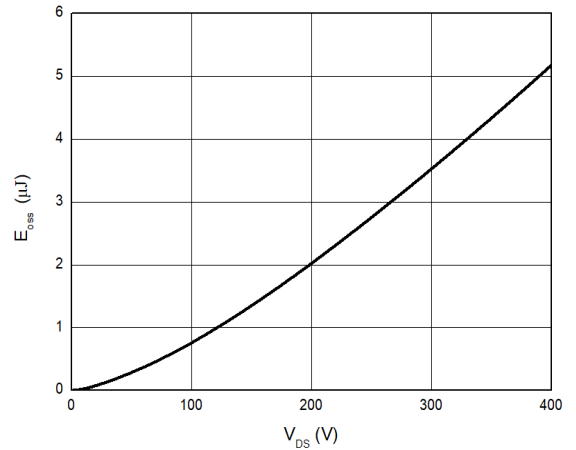


Figure 8. Typical C_{OSS} Stored Energy



Typical Characteristics

$T_j=25^\circ\text{C}$ unless otherwise stated

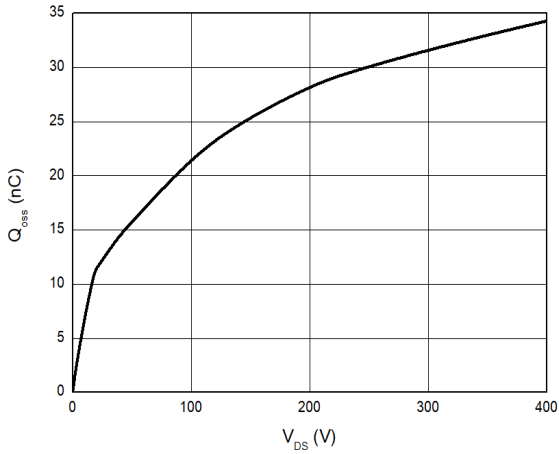


Figure 9. Typical Q_{oss}

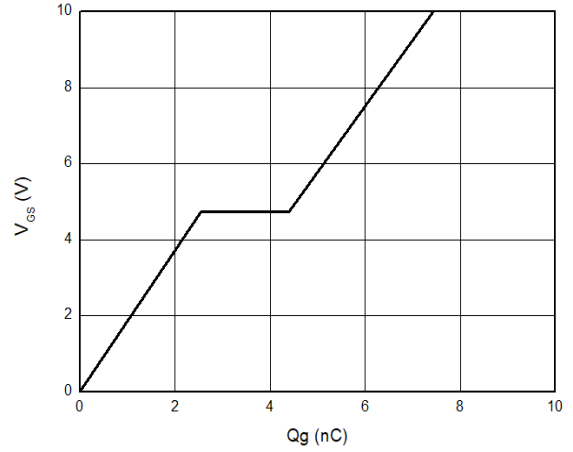


Figure 10. Typical Gate Charge ($V_{DS}=400\text{V}$, $I_D=1\text{A}$)

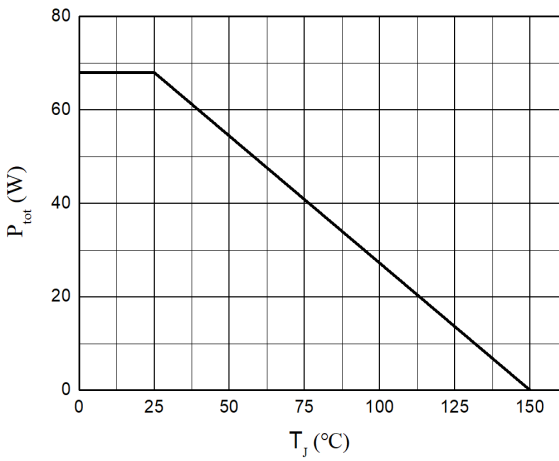


Figure 11. Power Dissipation

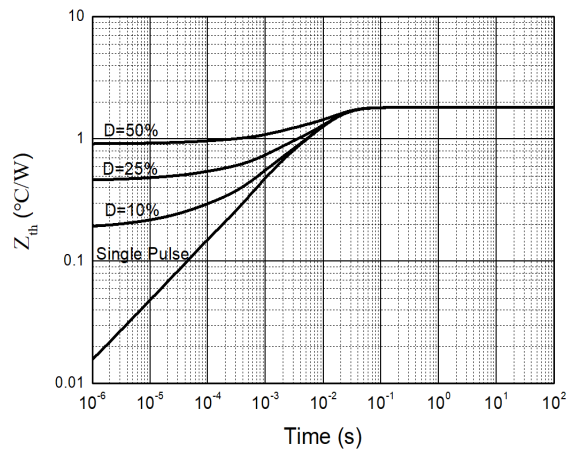


Figure 12. Transient Thermal Resistance



Typical Characteristics

T_J=25°C unless otherwise stated

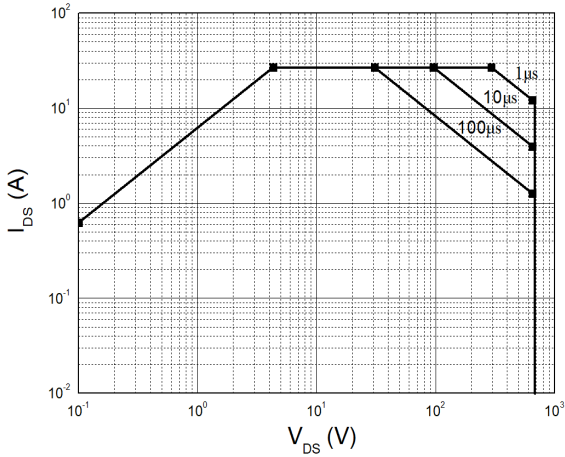


Figure 13. Safe Operating Area T_J=25°C

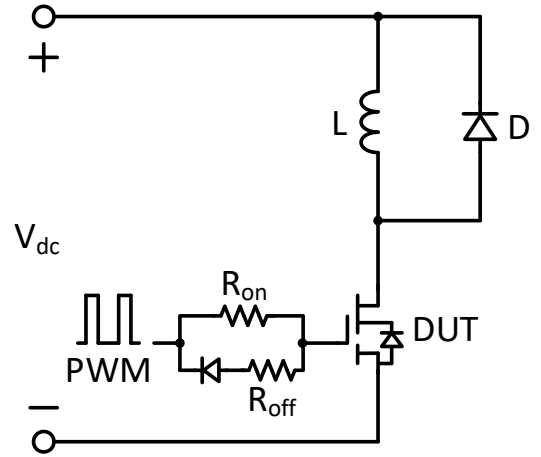


Figure 14. Switching times with inductive load

V_{DS}=400V, V_{GS}=0V to 10V, I_D=2.1A,
 R_{G-on(ext)}=6.8Ω, R_{G-off(ext)}=2.2Ω, L=250μH

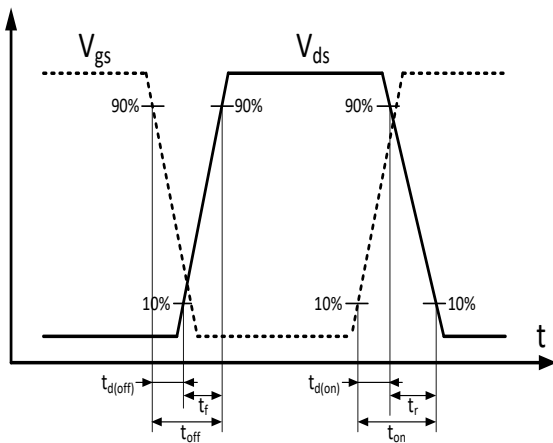
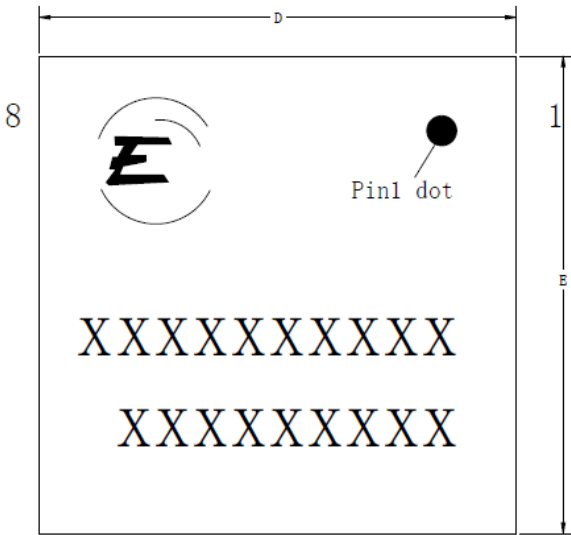


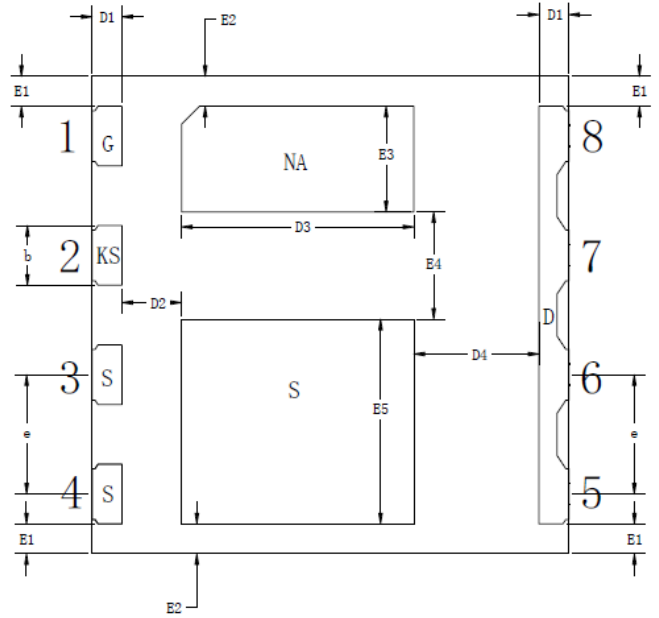
Figure 15. Switching times with waveform

PACKAGE DIMENSIONS

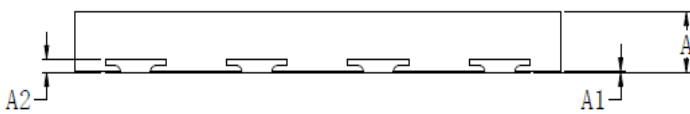
TOP VIEW



BOTTOM VIEW



Side View(left/right)



Symbol	Min. (mm)	Mean. (mm)	Max. (mm)
A	0.850	0.900	0.950
A1	0.000	0.020	0.050
A2	0.203REF		
D	7.900	8.000	8.100
E	7.900	8.000	8.100
D1	0.400	0.500	0.600
D2	0.900	1.000	1.100
D3	3.800	3.900	4.000
D4	2.000	2.100	2.200
E1	0.400	0.500	0.600
E2	0.400	0.500	0.600
E3	1.670	1.770	1.870
E4	1.700	1.800	1.900
E5	3.330	3.430	3.530
b	0.900	1.000	1.100
e	1.900	2.000	2.100



CE65H160DNXI

Revision history

Major changes since the last revision

Revision	Date	Description of changes
1.0	2023-12-25	Initial release